Linear MIMO Equalization for High-Speed Chip-to-Chip Communication

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***Abstract*—In this contribution, we present a linear multiple-input multiple-output (MIMO) equalization scheme at the receiver side for high-speed electrical chip-to-chip communication. As opposed to traditional single-input single-output (SISO) equalization per lane, this MIMO approach enables cooperating receivers to treat crosstalk (XT) between neighboring channels as an information-bearing signal instead of a disturbing signal, allowing to mitigate both inter symbol interference and XT. Given a simulated 4×4 MIMO electrical chip-to-chip interconnect channel, we point out that, for a given total number of equalizer taps, MIMO equalization can outperform SISO equalization. Moreover, by further increasing the total number of equalizer taps, MIMO equalization allows to obtain performance gains that are substantially larger than for SISO equalization.**

I. Introduction

In order to keep up with the increasing processing speed of integrated circuits (ICs), the bit rates supported by chip-to-chip interconnects must grow at the same pace. Typically, an electrical chip-to-chip interconnect consists of L parallel lanes connecting L transmitters at the transmitter chip to L receivers at the receiver chip. Increasing bit rates and associated signal bandwidths, however, cause current chip-to-chip interconnects to suffer from high-frequency attenuation, caused by skin effect and dielectric loss, which gives rise to inter symbol interference (ISI). When pushing communication speeds into the multi-Gbps range, sophisticated channel equalization is required to compensate for the ISI, which not only complicates tuning the equalization parameters but could also violate system power and chip area constraints. Using Tomlinson-Harashima precoding (THP) or decision feedback equalization (DFE), data rates near 10 Gbps per lane are currently being achieved with a power consumption of about 1 mW/Gbps [1]–[5]. Recent research (e.g., [6]–[8]) deals with increasing this speed up to 25 Gbps per lane, whereas in the (near) future speeds up to 100 Gbps per lane are targeted [9].

In addition to ISI, crosstalk (XT) originating from mutual coupling between neighboring wires further decreases the performance of multiconductor chip-to-chip interconnects. Due to growing data rates and reduced circuit dimensions, increased XT is expected to considerably deteriorate the performance of future multi-Gbps equalization schemes. Moreover, since XT is commonly treated as additional noise and not compensated for, it is considered a potential bottleneck for further increasing the bit rates over electrical chip-to-chip interconnects.

In this paper, we present a linear multiple-input multiple-output (MIMO) post-equalization scheme for high-speed electrical chip-to-chip communication. As opposed to traditional single-input single-output (SISO) equalization per lane, MIMO equalization allows cooperating receivers to treat XT from neighboring channels as an information-bearing signal, turning XT from a limiting into a beneficial factor. The potential of MIMO pre-equalization using THP has been shown in [10], where non-linear MIMO equalization is used to improve the reliability of 10 Gbps Ethernet over unshielded twisted-pair (UTP) cables, also known as 10GBASE-T. We propose a MIMO equalization scheme in which the mean square error (MSE) between the equalizer outputs and the corresponding data symbols is minimized. In this way, the resulting minimum mean square error (MMSE) MIMO equalization scheme is able to tackle ISI and XT simultaneously, which is shown to significantly improve the error rate performance with respect to linear SISO equalization.

II. System model

Fig. 1 displays a baseband communication system representing a typical electrical chip-to-chip interconnect consisting of L transmitters and L receivers which are connected by L parallel lanes. Each of the L transmitters applies its real-valued data symbol stream $\{a^{(l)}(k)\}$, with $1 \leq l \leq L$, to a pulse shaping filter $H_{\mathrm{tr}}(f)$ at a symbol rate $1/T$. The symbol streams are assumed to be spatially and temporally independent, i.e., $E\left[a^{(l_1)}(k_1)\, a^{(l_2)}(k_2)\right] = \sigma_a^2 \delta_{l_1-l_2} \delta_{k_1-k_2}$, such that the average energy transmitted per symbol is given by

$$E_{\mathrm{s}} = \sigma_a^2 \int_{-\infty}^{+\infty} |H_{\mathrm{tr}}(f)|^2 \, \mathrm{d}f \qquad (1)$$

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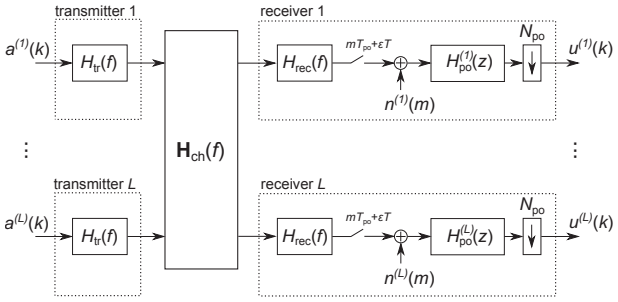

Figure 1. SISO Equalization scheme.

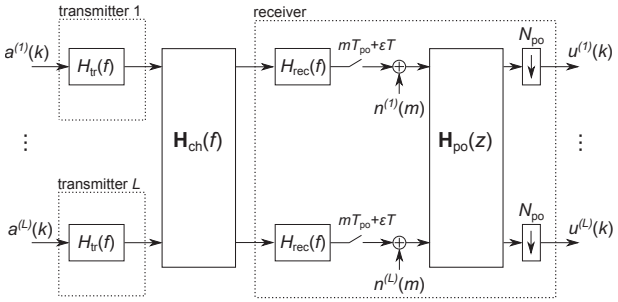

Figure 2. MIMO Equalization scheme.

The L channels between the transmitters and the receivers along with the XT channels are captured by the channel matrix $\mathbf{H}_{\rm ch}(f)$; the (r,p)-th entry $H_{\rm ch}^{(r,p)}(f)$ denotes the channel response between the p-th transmitter and the r-th receiver, with $1 \le r,p \le L$. The L received signals, affected by channel dispersion and XT, are each filtered by an analog receiver filter $H_{\rm rec}(f)$ and sampled at (a multiple of) the symbol rate $1/T_{\rm po} = N_{\rm po}/T$; note that the sampling instants $\{mT_{po} + \varepsilon T\}$ depend on the sampling phase ε. The stationary noise at the receiver is represented by the additive noise samples $n^{(1)}(m), \ldots, n^{(L)}(m)$. In the SISO equalization scheme from Fig. 1, each of the L receivers is equipped with a linear discrete-time equalizer filter $H_{\rm po}^{(l)}(z)$, with $1 \le l \le L$, where $H_{\rm po}^{(l)}(z)$ is the z-transform of the equalizer's impulse response $h_{\rm po}^{(l)}(m)$:

$$H_{\rm po}^{(l)}(z) = \sum_m h_{\rm po}^{(l)}(m)\, z^{-m}. \tag{2}$$

The outputs of the equalizer filters are downsampled by a factor $N_{\rm po}$, yielding the rate 1/T sequences $\{u^{(l)}(k)\}$, with $1 \le l \le L$, based on which the symbol decisions are taken. The equalizer filters in the SISO scheme from Fig. 1 intend to mitigate the ISI present in the received samples; they are not able to benefit from XT contributions captured by the other receivers. Hence, XT can be treated only as a disturbing signal, along with the additive noise signals.

In order to exploit the spatial diversity offered by the XT channels, we propose the MIMO post-equalization scheme displayed in Fig. 2. Receiver cooperation is implemented by introducing an equalization matrix $\mathbf{H}_{\rm po}(z)$ consisting of $L \times L$ equalizer filters; the (r,p)-th entry $H_{\rm po}^{(r,p)}(z)$ represents the equalizer filter linking the p-th input of the equalization matrix with the r-th output, with $1 \le r,p \le L$. If the off-diagonal equalizer filters $H_{\rm po}^{(r,p)}(z) = 0$ with $r \ne p$, the MIMO system from Fig. 2 degenerates to the SISO system from Fig. 1.

III. MMSE MIMO Equalization

Under the assumption that the sequences $\{g^{(q,p)}(m)\}$, with $1 \le q,p \le L$, are obtained by sampling at instants $\{mT_{po}+\varepsilon T\}$ the impulse responses of the corresponding cascades $H_{\rm tr}(f)H_{\rm ch}^{(q,p)}(f)H_{\rm rec}(f)$, the outputs $\{u^{(l)}(k)\}$ of the MIMO equalization scheme, with $1 \le l \le L$, are readily verified to be given by

$$u^{(l)}(k) = \sum_{p=1}^{L}\sum_m h^{(l,p)}(m)\, a^{(p)}(k-m) + \sum_{p=1}^{L}\sum_m h_{\rm po}^{(l,p)}(m)\, n^{(p)}(kN_{\rm po}-m), \tag{3}$$

where

$$h^{(l,p)}(m) = \sum_{q=1}^{L}\sum_{m_1} h_{\rm po}^{(l,q)}(m_1)\, g^{(q,p)}(mN_{\rm po}-m_1). \tag{4}$$

Ideally, when no noise, ISI or XT occurs, we should have $u^{(l)}(k) = a^{(l)}(k)$, for $1 \le l \le L$.

In the case of practical equalizers with a limited number of $L_{\rm po} = L_{\rm po,min} + L_{\rm po,max} + 1$ non-zero filter coefficients $\{h_{\rm po}^{(r,q)}(m)\}$, with $m = -L_{\rm po,min}, \ldots, L_{\rm po,max}$, matrix notation can be used for the sake of notational simplicity. To this end, we introduce the $L \times (LL_{\rm po})$ block matrix $\overline{\mathbf{H}}_{\rm po}$ comprising all equalizer coefficients

$$\overline{\mathbf{H}}_{\rm po} = \left[\breve{\mathbf{H}}_{\rm po}(-L_{\rm po,min}), \ldots, \breve{\mathbf{H}}_{\rm po}(L_{\rm po,max})\right], \tag{5}$$

where the (l,q)-th entry of the $L \times L$ matrix $\breve{\mathbf{H}}_{\rm po}(m)$ is given by $h_{\rm po}^{(l,q)}(m)$. Similarly, we introduce the $(LL_{\rm po}) \times L$ block matrix $\overline{\mathbf{G}}(m)$ as

$$\overline{\mathbf{G}}(m) = \begin{bmatrix} \breve{\mathbf{G}}\,(mN_{\rm po} + L_{po,min}) \\ \vdots \\ \breve{\mathbf{G}}\,(mN_{\rm po} - L_{\rm po,max}) \end{bmatrix}, \tag{6}$$

where the (q,p)-th entry of the $L \times L$ matrix $\breve{\mathbf{G}}(m)$ is given by $g^{(q,p)}(m)$. Defining the $(LL_{\rm po})$-dimensional column vector $\overline{\mathbf{n}}(m)$ as

$$\overline{\mathbf{n}}(m) = \begin{bmatrix} \breve{\mathbf{n}}(mN_{\rm po} + L_{\rm po,min}) \\ \vdots \\ \breve{\mathbf{n}}(mN_{\rm po} - L_{\rm po,max}) \end{bmatrix}, \tag{7}$$

with the p-th element of $\breve{\mathbf{n}}(m)$ being given by $n^{(p)}(m)$, and introducing the L-dimensional column vectors $\mathbf{a}(k)$

and $\mathbf{u}(k)$, the l-th elements of which are given by $a^{(l)}(k)$ and $u^{(l)}(k)$, respectively, it follows that equations (3) and (4) can be written as

$$\mathbf{u}(k) = \sum_m \mathbf{H}(m)\,\mathbf{a}(k-m) + \overline{\mathbf{H}}_{\rm po}\overline{\mathbf{n}}(k), \qquad (8)$$

and

$$\mathbf{H}(\mathrm{m}) = \overline{\mathbf{H}}_{\rm po}\overline{\mathbf{G}}(m), \qquad (9)$$

respectively. According to (8) and (9), the error vector $\mathbf{e}(k) = \mathbf{u}(k) - \mathbf{a}(k)$ between the actual output $\mathbf{u}(k)$ and the target output $\mathbf{a}(k)$ is given by

$$\mathbf{e}(k) = \sum_m \left(\mathbf{H}(m) - \delta_m\,\mathbf{I}_L\right)\,\mathbf{a}(k-m) + \overline{\mathbf{H}}_{\rm po}\overline{\mathbf{n}}(k). \qquad (10)$$

As a performance measure for the proposed equalization scheme, we introduce the normalized mean square error (MSE) caused by noise, ISI, and XT:

$$\mathrm{MSE} \triangleq \frac{E\left[\|\mathbf{e}(k)\|^2\right]}{E\left[\|\mathbf{a}(k)\|^2\right]}. \qquad (11)$$

From (10), it follows that the MSE (11) reduces to

$$\mathrm{MSE} = \frac{1}{L\sigma_a^2}\left[\sigma_a^2 \sum_m \left\|\overline{\mathbf{H}}_{\rm po}\overline{\mathbf{G}}(m) - \delta_m\,\mathbf{I}_L\right\|^2 + \mathrm{tr}\left(\overline{\mathbf{H}}_{\rm po}\mathbf{R}_{\overline{\mathbf{n}}}\overline{\mathbf{H}}_{\rm po}^{\rm T}\right)\right], \qquad (12)$$

where the superscript T denotes matrix transpose and the $(LL_{\rm po}) \times (LL_{\rm po})$ autocorrelation matrix $\mathbf{R}_{\overline{\mathbf{n}}}$ is defined as

$$\mathbf{R}_{\overline{\mathbf{n}}} \triangleq E\left[\overline{\mathbf{n}}(m)\,\overline{\mathbf{n}}(m)^{\rm T}\right]. \qquad (13)$$

Let us assume that the sequences $\{g^{(q,p)}(m)\}$ have limited time duration, i.e., $g^{(q,p)}(m) = 0$ for $m \notin (-L_{g,\min}, L_{g,\max})$ and for all q and p. In this way, the number of non-zero matrices $\overline{\mathbf{G}}(m)$ is limited to the interval $(-L_{\rm G,min}, L_{\rm G,max})$, where

$$\begin{cases} L_{\rm G,min} = \left\lfloor \frac{L_{g,\min}+L_{\rm po,min}}{N_{\rm po}} \right\rfloor \\ L_{\rm G,max} = \left\lfloor \frac{L_{g,\max}+L_{\rm po,max}}{N_{\rm po}} \right\rfloor \end{cases} \qquad (14)$$

By applying a number of matrix manipulations to (12), the minimum mean square error (MMSE) post-equalization scheme $\overline{\mathbf{H}}_{\rm po,MMSE}$ minimizing the MSE between the actual output vector $\mathbf{u}(k)$ and the target output vector $\mathbf{a}(k)$, and, hence, mitigating both ISI and XT, can be shown to be elegantly expressed as

$$\overline{\mathbf{H}}_{\rm po,MMSE} = \overline{\mathbf{G}}(0)^{\rm T}\mathbf{A}^{-1}, \qquad (15)$$

where

$$\mathbf{A} \triangleq \sum_{m=-L_{\rm G,min}}^{L_{\rm G,max}} \overline{\mathbf{G}}(m)\overline{\mathbf{G}}(m)^{\rm T} + \frac{1}{\sigma_a^2}\mathbf{R}_{\overline{\mathbf{n}}}. \qquad (16)$$

By substituting (15) in (12), the MMSE is shown to reduce to

$$\mathrm{MMSE} = \frac{1}{L}\,\mathrm{tr}\left(\mathbf{I}_L - \mathbf{G}(0)^{\rm T}\mathbf{A}^{-1}\mathbf{G}(0)\right). \qquad (17)$$

A. No crosstalk

In the absence of XT, i.e., $H_{\rm ch}^{(r,p)}(f) = 0$ for $r \neq p$, the MMSE MIMO equalization scheme (15) is easily shown to reduce to the traditional SISO equalization scheme from Fig. 1, provided that the additive noise samples are spatially uncorrelated, i.e., $E\left[n^{(p_1)}(l_1)\,n^{(p_2)}(l_2)\right] = 0$ if $p_1 \neq p_2$. As a result, the MSE at the output of the l-th SISO equalizer reduces to

$$E\left[\left|\mathbf{e}^{(l)}(k)\right|^2\right] = \sigma_a^2 \sum_m \left|\mathbf{h}_{\rm po}^{(l,l)}\mathbf{g}^{(l,l)}(m) - \delta_m\right|^2 + \mathbf{h}_{\rm po}^{(l,l)}\mathbf{R}_{\overline{\mathbf{n}}}^{(l)}\left(\mathbf{h}_{\rm po}^{(l,l)}\right)^{\rm T}, \qquad (18)$$

where the vectors $\mathbf{g}^{(q,p)}(m)$ and $\mathbf{h}_{\rm po}^{(l,q)}$ are defined as

$$\mathbf{g}^{(q,p)}(m) = \begin{bmatrix} g^{(q,p)}(mN_{\rm po} + L_{\rm po,min}) \\ \vdots \\ g^{(q,p)}(mN_{\rm po} - L_{\rm po,max}) \end{bmatrix}, \qquad (19)$$

$$\mathbf{h}_{\rm po}^{(l,q)} = \left[h_{\rm po}^{(l,q)}(-L_{\rm po,min}), \ldots, h_{\rm po}^{(l,q)}(L_{\rm po,max})\right], \qquad (20)$$

and the (l_1, l_2)-th element of the $L_{\rm po} \times L_{\rm po}$ matrix $\mathbf{R}_{\overline{\mathbf{n}}}^{(l)}$ is given by

$$\left(\mathbf{R}_{\overline{\mathbf{n}}}^{(l)}\right)_{l_1,l_2} = E\left[n^{(l)}(l_2)\,n^{(l)}(l_1)\right]. \qquad (21)$$

From the definition (11), it follows that the total normalized MSE can be obtained as

$$\mathrm{MSE} \triangleq \frac{1}{L\sigma_a^2}\sum_l E\left[\left|\mathbf{e}^{(l)}(k)\right|^2\right], \qquad (22)$$

which according to (18) is minimized by selecting the SISO equalizers $\mathbf{h}_{\rm po,MMSE}^{(l,l)}$ as

$$\mathbf{h}_{\rm po,MMSE}^{(l,l)} = \mathbf{g}^{(l,l)}(0)^{\rm T}\left(\mathbf{B}^{(l)}\right)^{-1}, \qquad (23)$$

where the $L_{\rm po} \times L_{\rm po}$ matrix $\mathbf{B}^{(l)}$ is given by

$$\mathbf{B}^{(l)} = \sum_{m=-L_{\rm G,min}}^{L_{\rm G,max}} \mathbf{g}^{(l,l)}(m)\,\mathbf{g}^{(l,l)}(m)^{\rm T} + \frac{1}{\sigma_a^2}\mathbf{R}_{\overline{\mathbf{n}}}^{(l)}. \qquad (24)$$

B. MMSE SISO equalization

In order to obtain a fair comparison between SISO and MIMO equalization, we derive the MMSE SISO equalization scheme for a general MIMO channel including XT. In this way, the MSE at the output of the

l-th equalizer can be shown to reduce to

$$E\left[\left|\mathbf{e}^{(l)}(k)\right|^2\right] = \sigma_a^2 \sum_m \left[\left|\mathbf{h}_{\mathrm{po}}^{(l,l)}\mathbf{g}^{(l,l)}(m) - \delta_m\right|^2 + \sum_{p\neq l}\left|\mathbf{h}_{\mathrm{po}}^{(l,l)}\mathbf{g}^{(l,p)}(m)\right|^2\right] + \mathbf{h}_{\mathrm{po}}^{(l,l)}\mathbf{R}_{\overline{\mathbf{n}}}^{(l)}\left(\mathbf{h}_{\mathrm{po}}^{(l,l)}\right)^{\mathrm{T}}. \quad (25)$$

Taking the similarity between (25) and (18) into account, it is readily verified that (25) and hence (22) are minimized by selecting the SISO equalizers $\mathbf{h}_{\mathrm{po,MMSE}}^{(l,l)}$ as follows:

$$\mathbf{h}_{\mathrm{po,MMSE}}^{(l)} = \mathbf{g}^{(l,l)}(0)^{\mathrm{T}}\left(\tilde{\mathbf{B}}^{(l)}\right)^{-1}, \quad (26)$$

where

$$\tilde{\mathbf{B}}^{(l)} = \sum_{m=-L_{\mathrm{G,min}}}^{L_{\mathrm{G,max}}} \mathbf{g}^{(l,l)}(m)\,\mathbf{g}^{(l,l)}(m)^{\mathrm{T}} + \frac{1}{\sigma_a^2}\tilde{\mathbf{R}}_{\overline{\mathbf{n}}}^{(l)}, \quad (27)$$

and

$$\tilde{\mathbf{R}}_{\overline{\mathbf{n}}}^{(l)} = \mathbf{R}_{\overline{\mathbf{n}}}^{(l)} + \sigma_a^2\left(\sum_{p\neq l}\sum_{m=-L_{\mathrm{G,min}}}^{L_{\mathrm{G,max}}} \mathbf{g}^{(l,p)}(m)\,\mathbf{g}^{(l,p)}(m)^{\mathrm{T}}\right). \quad (28)$$

Hence, it follows from the modified correlation matrix (28) that the MMSE SISO equalization scheme tackles XT originating from the off-diagonal channels $\mathbf{g}^{(l,p)}(m)$ with $p \neq l$ the same way it mitigates the additive noise.

IV. Numerical results

In this section, we illustrate the performance of the proposed MMSE MIMO post-equalization scheme on a 4×4 MIMO channel with strong XT, obtained from simulating an electrical chip-to-chip interconnect consisting of 4 adjacent stripline traces on a multilayer printed circuit board (PCB). We assume unit-energy square-root raised-cosine transmit and receive filters with 3 dB bandwidths $1/(2T)$ and $N_{\mathrm{po}}/(2T)$, respectively, and a roll-off factor $\beta = 0.3$ for both. The considered constellation is 2-PAM. Furthermore, the noise samples $n^{(l)}(m)$ are spatially and temporally independent real-valued zero-mean Gaussian random variables with variance $N_0/2$, i.e., $E\left[n^{(p_1)}(l_1)\,n^{(p_2)}(l_2)\right] = N_0/2\,\delta_{p_1-p_2}\delta_{l_1-l_2}$.

A. Infinite-length equalizers

To approximate the ideal case of infinite-length equalizer filters, we take $L_{\mathrm{po,min}} = L_{\mathrm{po,max}} = 100$, yielding for each equalizer filter a number of $L_{\mathrm{po}} = 201$ filter taps; we have verified that the obtained numerical results remain essentially the same when the number of taps is increased beyond 201. Under the assumption of symbol-spaced equalizer filters ($N_{\mathrm{po}} = 1$) and for $E_{\mathrm{s}}/N_0 = 20\,\mathrm{dB}$, we display in Fig. 3 the 1/MSE curves as a function of the sampling phase ϵ, for i) the MMSE SISO equalization scheme (23) in the absence of the XT, ii) the same (now suboptimal) SISO equalization scheme in the presence of XT, iii) the MMSE SISO equalization scheme (26), and iv) the MMSE MIMO equalization scheme (15). Here, it is assumed that when $\varepsilon = 0$, the impulse response corresponding to the frequency response $H_{\mathrm{tr}}(f)H_{\mathrm{ch}}^{(1,1)}(f)H_{\mathrm{rec}}(f)$ is sampled at the instant it reaches its maximum value. It is immediately apparent that the MSE performance of all equalization schemes depends on the sampling phase ε, which makes synchronization an important and critical task; this is due to the aliasing that occurs for symbol-rate sampling. The effect of aliasing is less pronounced when operating at $R_{\mathrm{b}} = 50$ Gbit/s per lane, because in this case the channel provides more attenuation to the frequency components in excess of $1/(2T)$. When considering the MSE performance of the traditional SISO equalization scheme (23) that ignores the presence of XT, we observe that for 10 Gbit/s per lane and $|\varepsilon| \leq 0.1$, the presence of XT (XT, suboptimal SISO equalization) gives rise to a degradation of almost 4 dB as compared to the case where XT is absent (no XT, MMSE SISO equalization). For $R_{\mathrm{b}} = 50$ Gbit/s, this degradation increases to at least 4.26 dB at $\varepsilon = 0.025$. By treating XT as additional Gaussian noise (XT, MMSE SISO equalization), the MMSE SISO equalization scheme manages to partially counteract the MSE degradation only at $R_{\mathrm{b}} = 50$ Gbit/s (providing about 1 dB gain in MSE performance); no MSE improvement is observed at $R_{\mathrm{b}} = 10$ Gbit/s since at relatively low bit rates the second term in (28) representing the XT is negligible with respect to the first term in (27) such that the suboptimal SISO equalization scheme (23) and the MMSE equalization scheme (26) yield the same equalization filters, despite the presence of XT. Contrary to the MMSE SISO equalization scheme, however, the MMSE MIMO equalization scheme does fully mitigate the impact of XT for

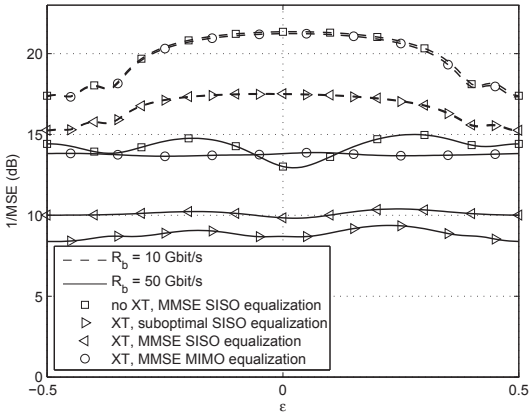

Figure 3. MSE for symbol-spaced SISO and MIMO equalizers of infinite length ($N_{\mathrm{po}} = 1$).

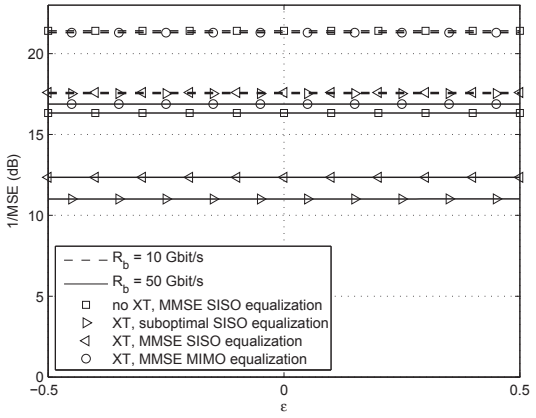

Figure 4. MSE for fractionally-spaced SISO and MIMO equalizers of infinite length ($N_{\mathrm{po}} = 2$).

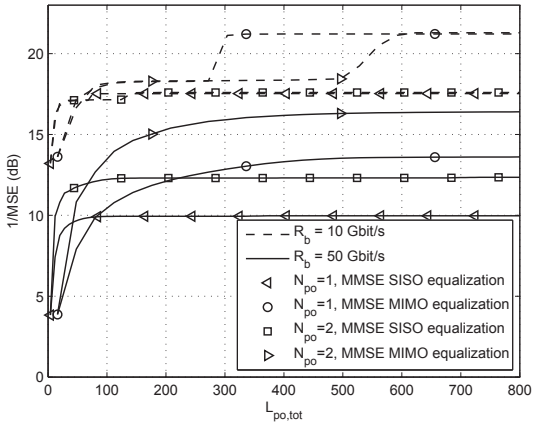

Figure 5. MSE for MMSE SISO and MIMO equalization schemes.

$R_{\mathrm{b}} = 10$ Gbit/s; its performance essentially coincides with that of the MMSE SISO equalization scheme in the absence of XT. When operating at $R_{\mathrm{b}} = 50$ Gbit/s, the MMSE MIMO equalizer yields an MSE performance that fluctuates around the MSE of the MMSE SISO equalization scheme in the absence of XT. Hence, for both bit rates the MMSE MIMO equalization scheme outperforms the MMSE SISO equalization scheme that treats XT as additional Gaussian noise by about 4 dB. However, as the number of equalizer filters is larger for MIMO equalization than for SISO equalization, this performance improvement comes at the cost of increased complexity.

In Fig. 4, we show the 1/MSE curves for the equalization schemes from Fig. 3 yet operating at twice the symbol rate ($N_{\mathrm{po}} = 2$). These so-called fractionally-spaced equalization schemes yield an MSE performance which is independent of the sampling phase, because no aliasing occurs within the frequency band $(-1.3/(2T), 1.3/(2T))$ that contains the transmitted signal. As sampling at twice the symbol rate satisfies the Nyquist-Shannon sampling theorem for the transmitted signal, no information is lost and all useful information on the transmitted signal is captured by the samples. Therefore, the resulting MSE performance is better than when sampling at the symbol rate, and cannot be improved by sampling at more than 2 samples per symbol. However, since symbol-spaced equalization with square-root Nyquist transmit and receive filters is known to be optimal on frequency-flat channels, the difference in performance between sampling at twice the symbol rate and sampling at the symbol rate using the optimum sampling phase will be small at low bit rates, where the channel can be considered approximately flat. Considering for instance the MMSE MIMO equalization scheme, it follows from Figs. 3 and 4 that the performance gain due to sampling at twice the symbol rate increases from only 0.06 dB at $R_{\mathrm{b}} = 10$ Gbit/s to 3 dB at $R_{\mathrm{b}} = 50$ Gbit/s. For (very) high bit rates, on the other hand, the high frequency components of the transmitted signal are largely suppressed by the channel, which reduces the impact of aliasing and again decreases the difference in performance between fractionally-spaced and symbol-spaced equalizers. In addition, the MMSE MIMO equalization scheme exploits the XT components that carry the useful data (hence improving equalizer performance) and suppresses the other XT components, which in the case of $R_{\mathrm{b}} = 50$ Gbit/s, results in a net performance gain of about 0.6 dB compared to the MMSE SISO equalization scheme in the absence of XT.

B. Finite-length equalizers

As the overall complexity of a particular SISO or MIMO equalization scheme can be characterized through the total number ($L_{\mathrm{po,tot}}$) of coefficients of all its equalization filters, we show in Fig. 5 the 1/MSE curves as a function of $L_{\mathrm{po,tot}}$, under the assumption that $\varepsilon = 0$. For SISO and MIMO equalization, $L_{\mathrm{po,tot}}$ is given by $4L_{\mathrm{po}}$ and $16L_{\mathrm{po}}$, respectively, with $L_{\mathrm{po,min}} = L_{\mathrm{po,max}}$. Although many filter taps are required to obtain optimal MSE performance, it follows from Fig. 5 that 20 to 30 coefficients per equalizer filter, corresponding to a total number of 80 to 120 coefficients for SISO equalization and 320 to 480 coefficients for MIMO equalization, are usually sufficient to achieve near optimal performance. For the MMSE MIMO equalizer with $N_{\mathrm{po}} = 2$ at $R_{\mathrm{b}} = 10$ Gbit/s, however, a total number of 600 filter coefficients are needed. Hence, to fully exploit the potential gain offered by MIMO equalization increased complexity is inevitable. Nonetheless, also for a given complexity, MIMO equalization is able to outperform its SISO counterpart. For instance, it follows from Fig. 5 that for given $L_{\mathrm{po,tot}}$, sampling at twice the symbol rate ($N_{\mathrm{po}} = 2$) always yields the best MSE performance in the case of $R_{\mathrm{b}} = 50$ Gbit/s and that fractionally-spaced

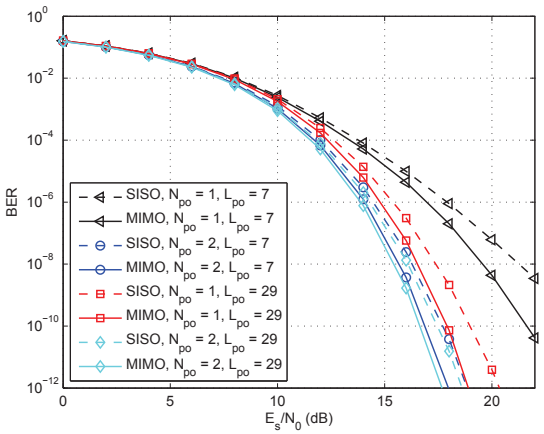

Figure 6. BER for MMSE SISO and MIMO equalization schemes operating at 50 Gbit/s per lane.

MIMO equalization is to be preferred over fractionally-spaced SISO equalization when the total number of filter coefficients exceeds 68. Hence, a MIMO scheme consisting of 16 filters of only 5 taps each is to be preferred over a SISO system with 20 taps per filter, although the complexity in terms of total number of filter coefficients is identical ($16\times5 = 4\times20 = 80$). Moreover, by increasing $L_{\mathrm{po,tot}}$ beyond 68, MIMO equalization allows to obtain performance gains that are substantially larger than for SISO equalization.

In Fig. 6, we show the BER versus E_s/N_0 for MMSE SISO and MIMO equalization schemes with $N_\mathrm{po} \in \{1, 2\}$ and $L_\mathrm{po} \in \{7, 29\}$ at a bit rate of $R_\mathrm{b} = 50$ Gbit/s per lane. Again we see that the equalization schemes operating at twice the symbol rate outperform the corresponding schemes operating at the symbol rate. For $N_\mathrm{po} = 2$, the MIMO scheme with $L_\mathrm{po} = 7$ outperforms the SISO scheme with $L_\mathrm{po} = 29$ by about 0.53 dB at a BER of 10^{-12}, although the total number of filter taps is (slightly) lower for the former scheme (16 x 7 = 112) than for the latter (4 x 29 = 116). Hence, in line with the conclusions from Fig. 5, MIMO equalization can improve the performance compared to SISO equalization, for a given total number of filter taps.

V. Conclusions

In this contribution, we presented a linear MIMO equalization scheme at the receiver side for multi-Gbps electrical chip-to-chip communication. By adopting this MIMO approach, the cooperating receivers consider XT from neighboring channels as an information-bearing signal, which significantly improves the MSE as well as the BER performance compared to SISO equalization. For both symbol-spaced and fractionally-spaced equalization schemes, it was shown that MIMO equalization allows to largely compensate for the performance loss due to XT and in some cases even manages to benefit from XT. Moreover, for a given total number of filter taps, MIMO equalization is shown to improve the MSE performance compared to SISO equalization, in spite of the smaller number of coefficients per individual filter of the MIMO equalizer.

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